Digital System Design

DE-31(CE)

I see a digital designer as an architect, who can invent interesting structures fulfilling functionality with creativity and effectiveness. The design needs to be flexible, scalable, reusable and testable. The main focus of the course is teaching students all the interesting elements of digital system design and the cost of inclusion of these elements in terms of power and area on the systems. This course covers a right mix of topics with colors of my personal experience in exploring and creating interesting and cost effective solution to complex design problems.

Credit Hours: 2-1

Instructor:

Dr. Shoab A. Khan

Email: kshoab@yahoo.com

TA:

Text Books:

Selected Chapters from the following:

1. Digital Design of Signal Processing Systems by Shoab Khan, John Wiley & Sons

Refrences:

1. Verilog HDL-A guide to digital design and synthesis by Samir Palnitkar, Prentice Hall Publisher
2. Advanced Digital Design with Verilog HDL by Michael D. Ciletti, Prentice Hall Pulisher

Objectives:

The objective of the course is to teach students

1. Verilog as hardware description language
2. FPGA architecture and logic Synthesis concept
3. Architecture of basic building blocks, adders, multipliers, shifters
4. Converting floating-point algorithms design in Matlab to Fixed-point format
5. Effective HW mapping techniques: Fully parallel, Time-shared, micro-coded architectures
6. Designing State-machines based architecture

Pre-requisites by Topics

Digital Logic Design, Computer Architecture, Signals and Systems,

Topics

1. High-level digital design methodology using Verilog, Design, Implementation, and Verification, 6 hrs
2. Application requiring HW implementation, Floating-Point to Fixed-Point Conversion, 6 hrs
3. Architectures for Basic Building Blocks, Adder, Compression Trees, and Multipliers, 8 hrs
4. Transformation for high speed using pipelining, retiming, and parallel processing, 3 hrs
5. Dedicated Fully Parallel Architecture, Time shared Architecture, Hardwired State Machine based Design, Micro Program State Machine based Design, 8 hrs
6. FPGA-based design and logic synthesis, 2 hrs

Computer Usage:

Verilog Simulator, FPGA Logic Synthesis tools

Grading Criteria:

Quizzes 5% ,
Labs & assignments to be developed ALONE: 10-15%,
Final project, teams of 1-3 students: 10-15%,
One/Two sessionals: 25-30%,
Final: 35-50